ABSTRACT

An apparatus and method for DFT processing using prime factor algorithm (PFA) on a selected number P of midamble chip values received by a CDMA receiver, where P has a plurality M of relatively prime factors F, and the DFT process is divided into M successive F-point DFT processes. The P data values are retrieved from a single input port memory and selectively permuted by a controller into parallel caches to optimize factoring with associated twiddle factors stored in parallel registers. The permuted inputs are factored in two or more parallel PFA circuits that comprise adders and multipliers arranged to accommodate any size F-point DFT. The outputs of the PFA circuits are processed by consolidation circuitry in preparation for output permutation of the values which are sent to memory for subsequent DFT cycles.